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ABSTRACT

This manual describes the CALM TV graphics interface, a low-cost means of producing quality graphics on an ordinary TV. The system permits the output of data in graphic as well as alphanumeric form and the input of data from the face of the TV using a light pen. The integrated circuits required in the interface can be obtained from standard suppliers for under $200. Provided in this document is all the information needed to construct this interface and interface it to standard output ports on any computer. One particular hardware configuration is illustrated with the TV interface and is connected to an S-100 based Z-80 system. (BB)

LOW COST GRAPHICS

SECOND EDITION May 1978

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PREFACE

The CALM TV Graphics Interface provides a low cost means of producing quality graphics on an ordinary TV. This documentation provides all the information needed to construct this interface and interface it to standard output ports on any computer. One particular hardware configuration is illustrated with the TV interface and is connected to an S-100 based Z-80 system. Assembly level listings of utility software are available in a comparison report: "Low Cost Graphics Software."

Educators interested in building this interface can obtain the three printed circuit boards from our offices at cost. The integrated circuits required in the interface can be obtained from standard suppliers for under $200. We would be pleased to assist educators that need help in constructing or interfacing graphics hardware.

The results reported herein were partly supported by the National Science Foundation. Any opinions, findings, conclusions or recommendations expressed in this publication are those of the author and do not necessarily reflect the views of the National Science Foundation, nor the Technical Education Research Centers, Inc.

CREDITS

The work reported here was supported by NSF grants SED77-1116 and SED76-18872 and Technical Education Research Centers corporate research funds. The interface development was a team effort. It was designed by Alan Siggia. Printed circuit layout was performed by Tony Cote, Judith Chadwick and Andrew Woziniak. Paul Antonucci and the author modified and debugged it.

The interface has been student tested at Springfield Technical Community College as part of the Computer and Laboratory Mathematics (CLAM) project in classes taught by Roy Whitney, Hilton Abbott, Henry Salz and the author. System software has been written by Paul Antonucci, Bill Torcaso and Kevin Jordan.

Robert F. Tinker, Ph.D.
Cambridge, MA
May 1978

TABLE I

CALM TV GRAPHICS INTERFACE

SPECIFICATIONS

Resolution:	256 x 256 dot raster
Access time:	1.7 μsec to alter or read two dots
Erase:	Single instruction erases screen to light or dark in 17 ms.
Refresh Memory:	Built-in 8K bytes static RAM
Input:	19 TTL compatible lines
Power:	5V at 2.2A
Video Output:	Composite video. Non-interlaced. Separate data, blank and sync lines are also available.
Output to Computer:	16 three state TTL lines indicating the light pen location, 6 TTL status lines.
Alphanumerics:	Software generated. Z-80 programs available that write at 1200 baud. 24 lines of 40 characters.
Scroll:	Hardware scroll up or down, one line at a time with wraparound.

INTRODUCTION

The CALM TV graphics interface permits the output of data in graphic, as well as alphanumeric form, on a common household TV and the input of data from the face of the TV using a light pen. With the appropriate software support, this interface can serve as the only input/output device required for a small computer system.

The CALM interface was designed for education, although its features make it useful in a wide range of applications. For education applications, it was felt absolutely necessary to be able to have graphics capability at the lowest possible price. The low cost and ready availability of home TV's made that a natural choice for an output medium. Since 98% of all households in the United States own a TV, this choice opens the possibilities of continuing education and home study using computer assisted instruction.

Once the choice was made to utilize a home TV, the resolution of the system was rather well defined. For various technical reasons (bandwidth limitation in the IF stage and interface circuit difficulties), the actual resolution of most home TV's corresponds to between 200 and 300 dots in both the vertical and horizontal directions. Because 256 is a very convenient number (it is 8 bits or 2 hexadecimal digits) we decided to divide the screen into a matrix with 256 dots in both the vertical and horizontal directions.

The TV interface has a memory cell dedicated to each of the 256^2 possible dots on the surface of the TV. Each cell remembers whether a 1 or a 0 (corresponding to a light spot or a dark spot) should be displayed at the corresponding location on the surface of the TV. The interface has

the capability of examining or altering the contents of any one of these memory cells. With this capability, any pattern including letters and graphs, can be written on the surface of the TV.

Light Pen Operation

The contents of the memory in the interface is continually and automatically being transferred to the TV so that a continuous image is observed on the TV. As with any TV picture, the image is written one dot at a time, starting in the upper left hand corner and writing left to right, one line at a time, from the top to the bottom of the screen. While this happens quite quickly on a human time scale, it is moderately slow for modern computer circuitry. Thus, when a light-sensitive element at the tip of the light pen senses the proximity of the electron beam on the face of the TV, it interrogates the interface to determine the address of the cell then being written. This address is the coordinate of that point and is made availalbe as an output from the interface. In this way, the computer can determine the coordinate of the location of the light pen and use that information as input data.

Input Techniques

We plan to use the light pen as an extremely versatile input medium, using the technique of "menu selection." In this technique, the computer displays two or more choices for the operator to make and the student/operator responds by pointing at the desired choice with a light pen. The power of the light pen-TV combination can be seen through the following examples:

Typewriter mode. It is possible to display the letters of the alphabet and control characters on the screen and then use the light pen to

point at the desired letters. The designated letters then appear at the top of the screen to create an alphanumeric message. While this procedure may not be quite as fast as a typewriter keyboard, students seldom can type quickly and, even when they can, there are few applications when fast typing is important in instructional uses of the computer. This mode duplicates the function of a keyboard and hence makes it unnecessary to have a special keyboard.

Test administration. It is possible to display a multiple-choice question on the TV screen and have the student point at the appropriate answer with light pen. We have designed an entire system for computer managed instruction using this mode which, because of the low terminal cost, is much less expensive than any other way of giving a large number of students a large number of different tests.

Analog mode. It is possible to draw on the face of the TV one or more dials, which can be "rotated" by the light pen and used as analog input to the computer. Better still, a linear potentiometer can be simulated in the same manner. This is attractive in simulation problems and gaming that require analog input. Again, there is a tremendous cost saving because each new simulation or game does not require a special piece of hardware for an input.

INSTRUCTIONS AND USE

The TV graphics interface communicates with the host computer through 16 input lines, 16 output lines and 11 other control lines. The 16 lines from the interface into the computer give the X and Y coordinates of the light pen. When the students desire to signal the computer that the light pen is located at the desired position, s/he presses a button which forces BUTTON low.

The computer can then read the coordinates of the pen from these 16 lines.

The computer communicates with the TV graphics interface through 16 data lines. These lines have four possible interpretations:

1. They can simply instruct the graphics terminal to clear every one of the bits, which would result in a totally black screen.
2. They can instruct the interface to set everyone of the bits, resulting in a totally white screen.
3. They can tell the interface that the next word on these 16 input lines represents the new X and Y coordinates of an internal cursor.
4. They can be used to instruct the graphics interface to "crawl" as defined below.

The "crawl" instruction turns out to be the one most often used. To understand its operation, you have to realize that there is a cursor in the interface which remembers the address (X and Y coordinates) of one of the dots on the surface of the TV. A single 8 bit crawl instruction causes two things to happen: first, the interface may, but does not have to, set or clear the bit at the location of the cursor, and then secondly, the cursor is moved to one of the 8 adjacent dots. Since the crawl instruction requires only 8 bits, two crawl instructions can be loaded into the interface simultaneously over the 16 lines. Both crawl instructions are executed microsecond so that the interface is availalbe to accept the next input as quickly as the computer can generate it.

The contents of the memory in the interface can be accessed with the crawl instruction by not writing any new information in memory. When not writing, the contents of the memory cells at the two locations of the cursor

at the end of each of the two crawl instructions is available on two additional output lines from the TV interface.

The reader will note that there is no provision for the automatic generation of characters in the interface. All such generation must be done under software control. We have written programs for the LSI-11 and the Z-80 that will generate characters from an ASCII input.

The decision to dispense with a hardware character generator reflects the primary design philosophy of extreme low cost. In order to keep the cost down, whenever there was a choice of accomplishing a particular function with hardware or software, the decision was made to eliminate the hardware. This has the added benefit of giving the system increased flexibility.

The final feature of the interface is its ability to "scroll." As part of the crawl instruction, it is possible for the entire contents of the screen to move up or down one line. When scrolling, the topmost line reappears at the bottom. If this line is then earsed, an effect similar to the rolling of a platen on a typewriter to expose freas paper can be obtained.

INPUT/OUTPUT LINES

The following section describes all the electrical lines between the TV interface and the host computer. The major lines consist of 16 data lines D_0-D_{15} into the interface and 16 lines P_0-P_{15} from the interface that reflect the light pen coordinates. Other lines control the interface or its access to the computer.

I. INPUT DATA D_0-D_{15}

Input data word D_0-D_{15}

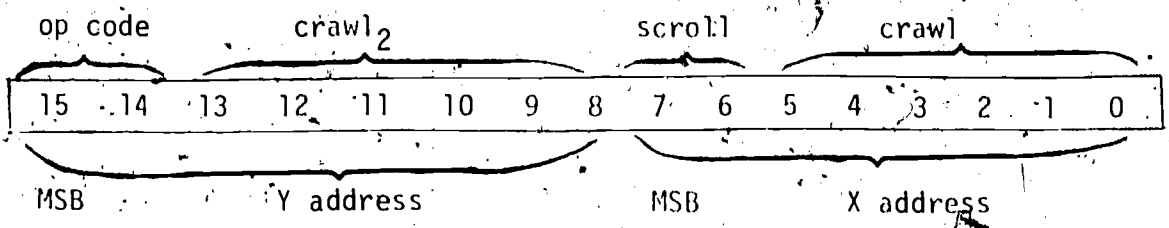


Figure I. Input data word.

A. If D_{15} D_{14} = 00 then the interface is in "crawl" mode and the remaining bits have the following significance in the order presented.

1. Scroll, if D_6 is set, the screen is scrolled up one line if D_7 if set, the screen is scrolled down one line.

2. Crawl, this causes a write, a read then a move.

a) Write - at the original cursor location, if memory is to be changed (i.e., light or dark displayed) then D_5 should be set to one to enable a memory change and D_4 should indicate the new dot intensity where 1 = set (opposite of background) or 0 = clear (same as background).

b) Read - the contents of the cell addressed by the current cursor value is read and brought out inverted on B_1.

c) Move - the cursor is next moved one element in any compass direction after writing by incrementing or decrementing each byte separately. Bits D_0-D_3 indicate direction

D_0 indicates west (i.e., left)

D_1 indicates east (i.e., right)

D_2 indicates south (i.e., down) (Unpredictable if used together)

D_3 indicates north (i.e., up)

D_0 or D_1 (but not both) can be used with D_2 or D_3 (but not both).

3. If D_8 -- D_{13} have the same significance as D_0 -- D_5 to create a second crawl instruction.

The crawl command structure is summarized in Figure 2.

Summary of crawl op code:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	0	Enable 12	Write I/O	N	S	E	W	Scroll Up	Scroll Dwn	Enable 4	Write I/O	N	S	E
		$Crawl_2$						$Crawl_1$						

Figure 2. Crawl command word.

B. If D_{15} D_{14} = 01 all other bits are ignored and the screen is set to all 1's (light). A busy signal is set = 0 while this happens. The background is now 1 (light) so that normal crawling instructions with bits 13 and 12 set cause black on white patterns.

C. If D_{15} and D_{14} = 10 all other bits are ignored and the screen is set to all 0's (blank). A busy signal is set = 0 while this happens. Background is set to 0 (dark) and white on black graphics can be generated.

D. If D_{15} D_{14} = 11 all other bits are ignored and the next signal on D_{15} -- D_0 indicates the new cursor address to be loaded into the graphics unit. No read or write is performed at the new location with this instruction. A subsequent crawl instruction can write at this location before moving to the next location. The origin of the X-Y corrdinates is in the lower left corner of the addressable screen. The X coordinate is in D_0 -- D_7 with D_7 the MSB. The Y coordinate is in D_8 -- D_{15} with D_{15} the MSB.

EXAMPLES

1. To draw a diamond centered at X = 128, Y = 128 that looks like Figure 3.

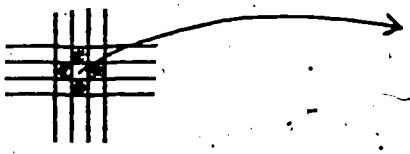


Figure 3. A diamond pattern

Go to 127, 128	1 1 x x x x x x	x x x x x x x
	1 0 0 0 0 0 0 0	0 1 1 1 1 1 1
Write a 1		
Crawl NE	0 0 1 1 0 1 1 0	0 0 1 1 1 0 1 0
Write a 1		
Crawl SE		
Write a 1		
Crawl SW	0 0 1 1 1 0 0 0	0 0 1 1 0 1 0 1
Write a 1		
Crawl N		

2. Go to 16_{10}, 200_{10} change its contents and examine the bit in 16,201

	1 1 x x x x x x	x x x x x x x	
	1 1 0 0 1 0 0 0	0 0 0 1 0 0 0 0	
Examine & don't move	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	
Write $\bar{B}_1$ and move N, Examine 16,201	0 0 0 0 0 0 0 0	0 0 1 B_1 0 0 0 0	inverted contents of 16,201 are on B_2

II. OTHER SIGNALS

A. DATA VALID. A positive transition on this input to the graphics unit indicates that the input data on D_0-D_{15} is valid. The interface will only then read these data and perform the indicated operation.

$\overline{VSYNC}$. Active low signal indicating that the TV is not writing because it is between picture scans. The crawl command results in ones or zeroes appearing on the screen while memory is being changed. The interface remembers whether the TV was last cleared to 0's ($D_{15}D_{14}$ = 10) or to 1's ($D_{15}D_{14}$ = 01). To disrupt the picture as little as possible, this value is written out during the crawl write cycle. If even this disruption is undesirable, crawls should be performed only when SYNC is low indicating that the TV is blanked.

C. $\overline{BUSY}$. This signal is zero while the screen is being cleared to zeroes or ones. No DATA VALID signal will be accepted while this is low.

D. $\overline{B}_1$, $\overline{B}_2$. Two bits which are set to the inverse of the contents of the screen locations reached at the end of each of the two crawl instructions.

E. P_0-P_{15}. Sixteen bit word giving the last X-Y address of the light pen. The format is the same as the input address, i.e., X is in P_0-P_7 with P_7 the MSB and Y is in P_8-P_{15} with P_{15} the MSB. This output is valid except for 30nsec while being updated. No update is possible while $\overline{SYNC}$ is low. These outputs are three-state and are enabled one byte at a time using $\overline{PXEN}$ and $\overline{PYEN}$.

F. $\overline{PXEN}$, $\overline{PYEN}$. Active low inputs that enable P_0-P_7(X) and P_8-P_{15} (Y) respectively.

G. PEN HIT. This line goes low when the light pen senses the electron beam.

CIRCUIT OPERATION

A simplified block diagram is shown in Figure 4; detailed schematics are shown in Figure 5.

The interface control mechanism spends most of its time addressing the 8K bytes of RAM to obtain the video information for the screen. Eight bits are pulled out every 1.33 microseconds and loaded into an 8 bit shift register IC 1. The data is then shifted out of this register at 6 MHz, formed into dots, blanked if necessary, inverted if the background bit is set, and then added to the sync signals at the output of IC 21. The low 5 bits of the memory address are derived from the horizontal counting circuit consisting of the three 74161's ICs 11 through 13. The 6 MHz signal is first divided by 8 at IC 13 to create the load logic every eighth bit. This is then divided by 47 to generate the horizontal flyback and blanking logic. The two counters, IC 11 and 12 accomplish this division. The logic presets the counter to -47. During counts -39 and -38 the horizontal sync signal is generated and the screen is blanked for a count below -32.

The remaining address is derived from the vertical counter which divides the horizontal sync signal by 266 in the 3 counters: IC 35,36, and 37. The resulting output pulse is at 59.999 Hz, sufficiently near the line frequency to give negligible interference. The ten counts above 256 generate the vertical sync signal and additional blanking. The 8 bits of vertical address that are generated in this counting chain are added to a

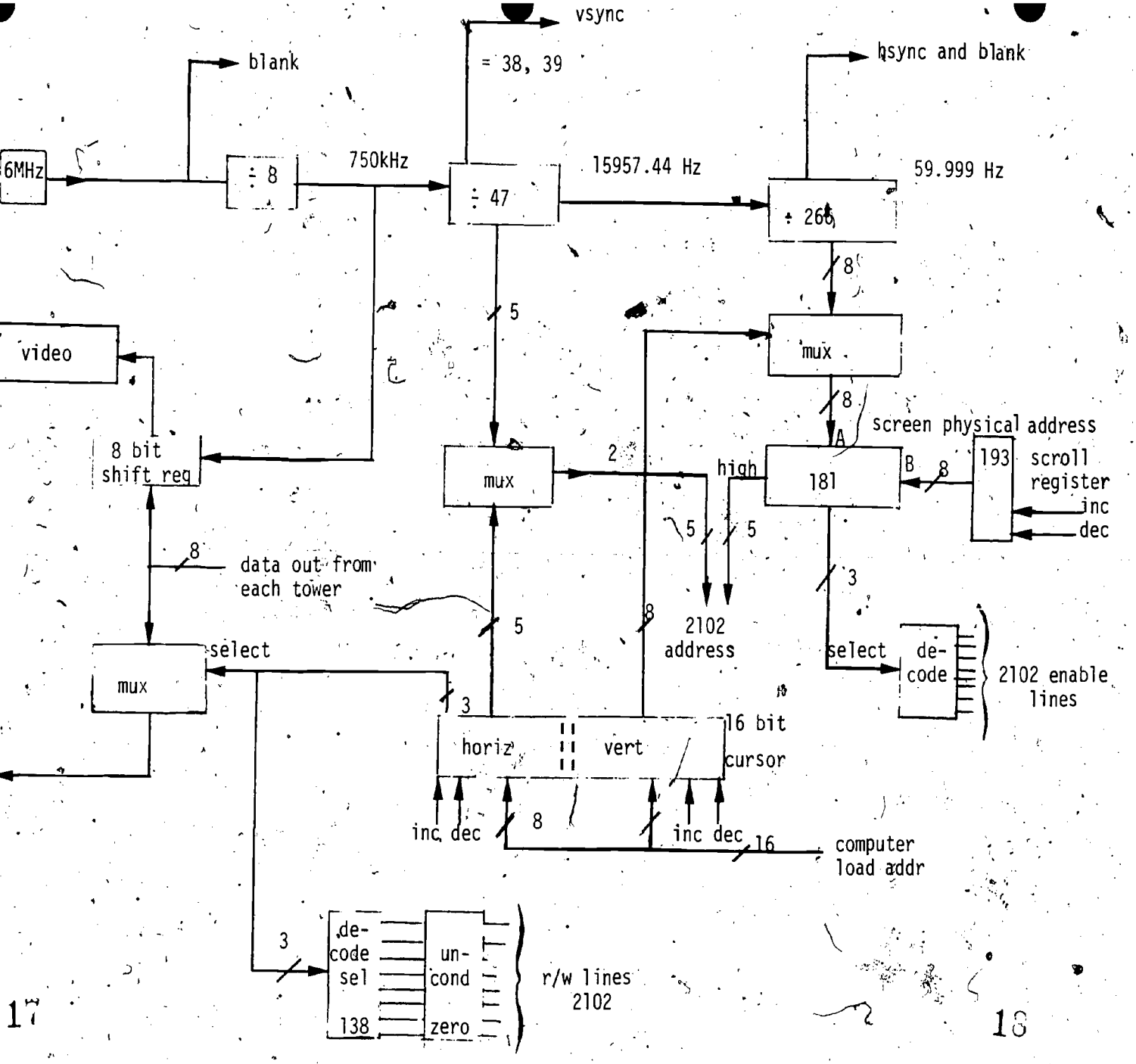
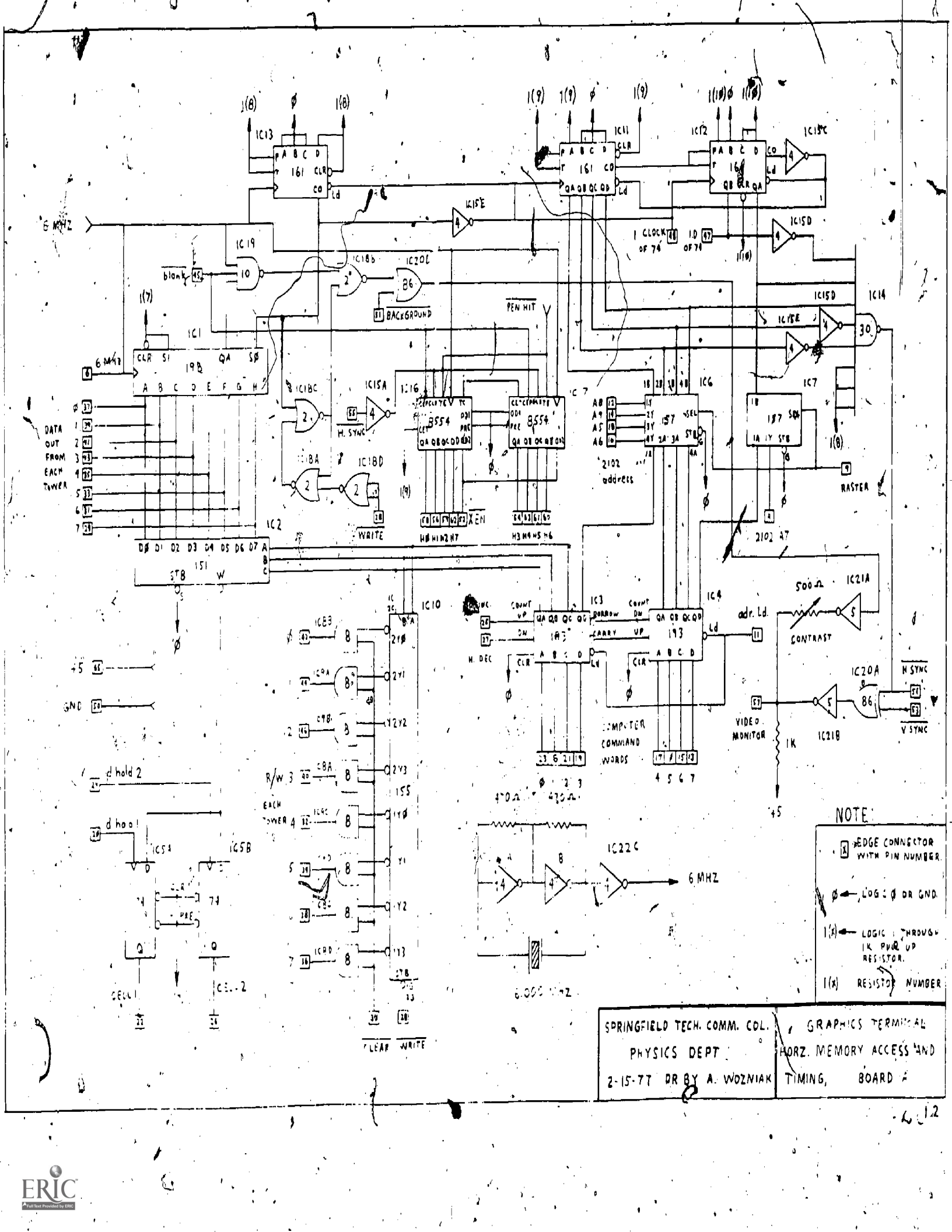
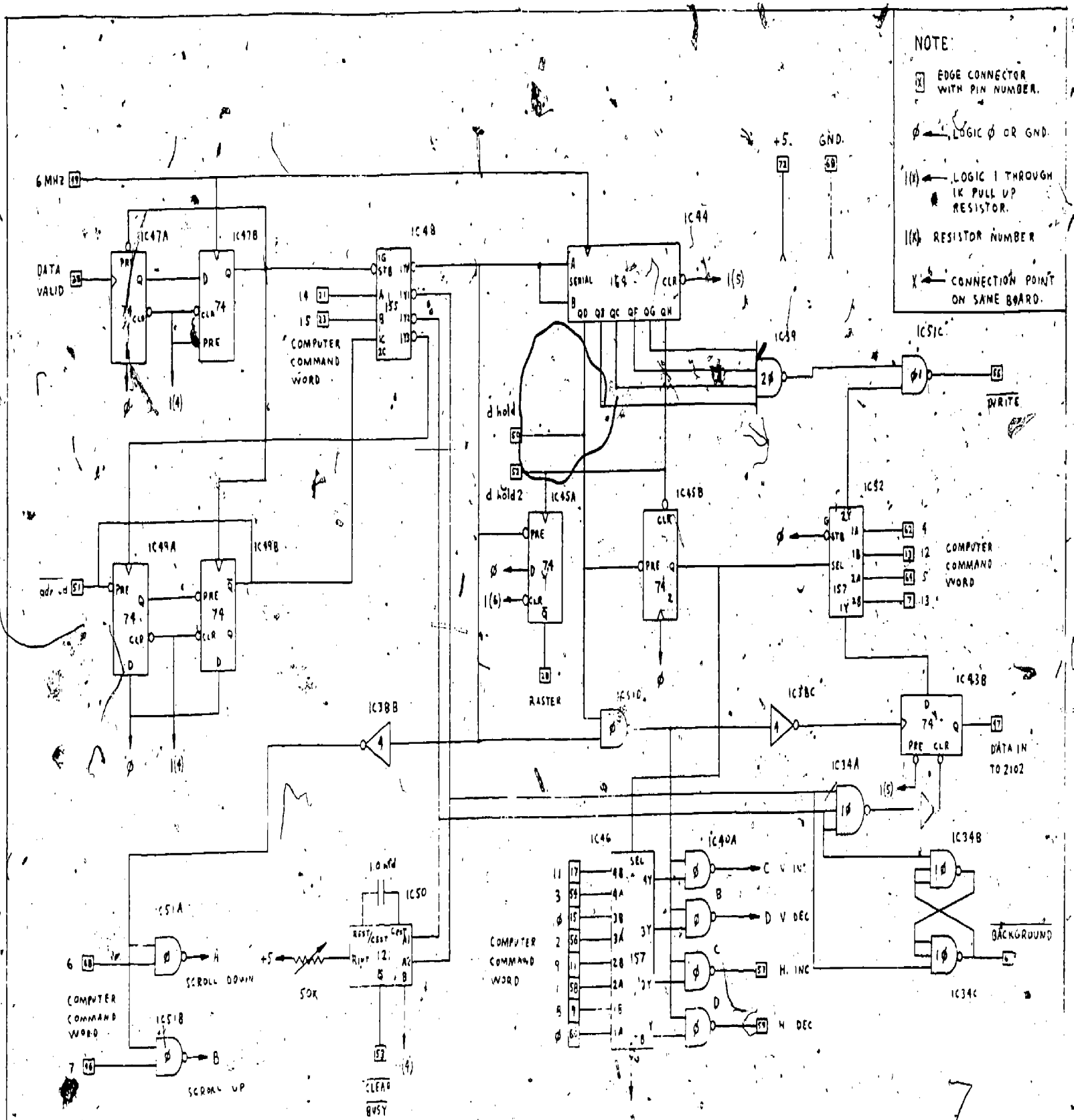


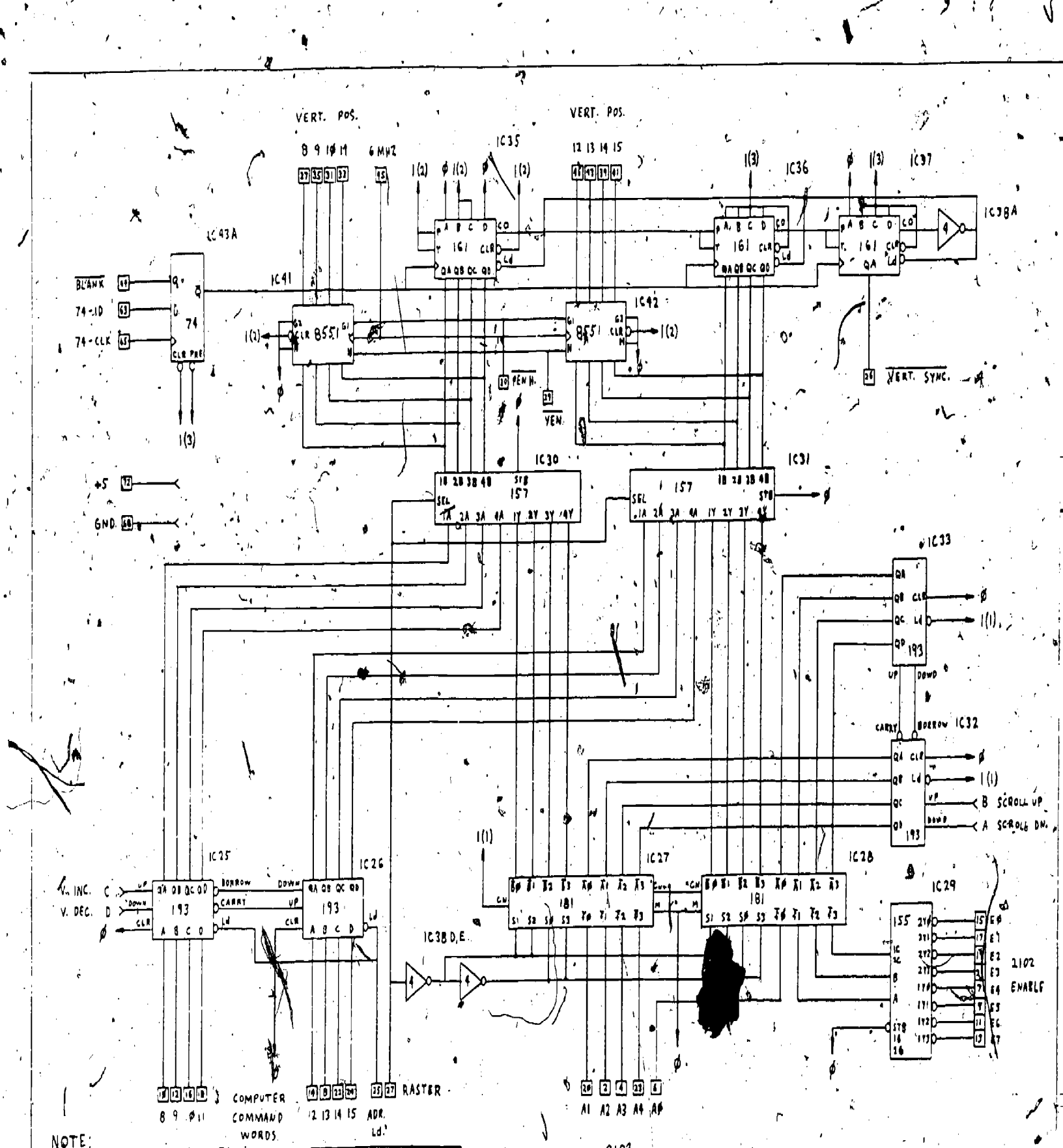
Figure 4. TV Interface Block Diagram



SPRINGFIELD TECH. COMM. COL. PHYSICS DEPT	GRAPHICS TERMINAL HORZ. MEMORY ACCESS AND TIMING, BOARD 2
2-15-77 DR BY A. WOZNIAK	



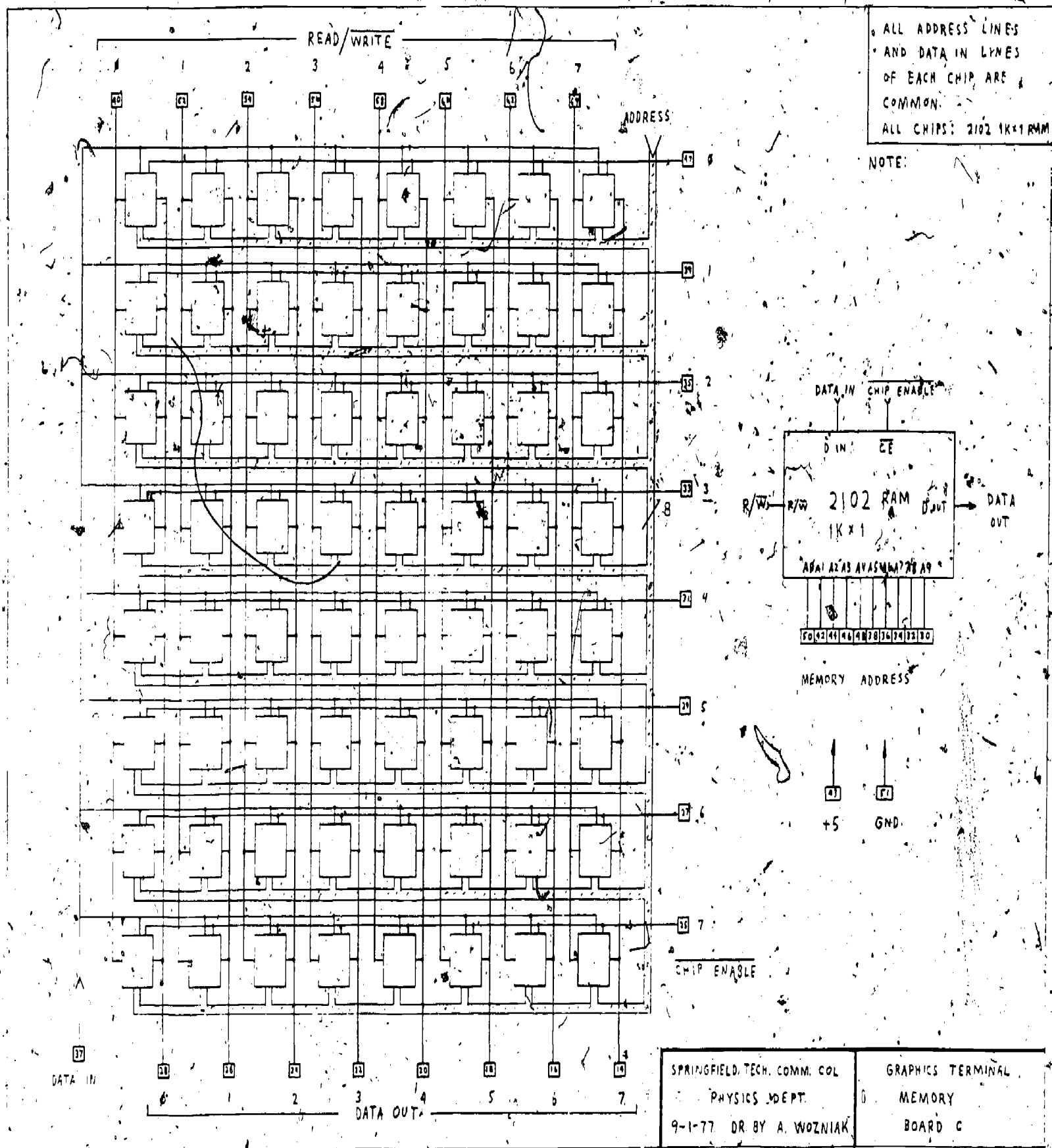
SPRINGFIELD TECH COMM COL PHYSICS DEPT 2-16-77 DR BY A POZIMAK	GRAPHICS TERMINAL COMPUTER INTERFACE AND CONTROL BOARD 5, PART A



NOTE:

- EDGE CONNECTOR WITH PIN NUMBER
- ∅ ← LOGIC ∅ OR GND.
- X > — CONNECTION POINT ON SAME BOARD.
- 1(x) ← LOGIC 1 THROUGH 1K PULL UP RESISTOR
- 1(x) RESISTOR NUMBER

SPRINGFIELD TECH. COMM. COL. PHYSICS DEPT. 2-22-77 DR. BY A. WOZNIAK	GRAPHICS TERMINAL VERT. MEMORY ACCESS AND TIMING, BOARD B, PART B


READ/WRITE
0 1 2 3 4 5 6 7
ADDRESS
DATA IN
0 1 2 3 4 5 6 7
DATA OUT
CHIP ENABLE
DATA IN
CHIP ENABLE
D IN
CE
R/W
2102 RAM
1K x 1
D OUT
DATA OUT
MEMORY ADDRESS
+5
GND
ALL ADDRESS LINES AND DATA IN LINES OF EACH CHIP ARE COMMON.
ALL CHIPS: 2102 1K x 1 RAM
NOTE:
SPRINGFIELD TECH. COMM. COL
PHYSICS DEPT.
9-1-77 DR BY A. WOZNIAK
GRAPHICS TERMINAL
MEMORY
BOARD C

scroll register which contains an arbitrary number which is incremented or decremented when each scroll instruction is executed.

The TV interface includes a hardware cursor which contains the address of one bit that may be modified or read. The address that is given to the RAMs can be derived from either this cursor or from the counting chain as determined by the set of multiplexers IC 6, 7, 30, and 31. The cursor resides in IC's 3,4, 25 and 26. The multiplexing of the vertical address is done before the scroll register is added so that the cursor is only addressing a physical line number under which a pattern may be scrolled. The cursor can read into an individual bit by enabling only one of the 8 read lines selected by the lowest three bits of the cursor address. This decoding is done in IC 10. When the screeen is cleared all the read/write lines are activated so that the screen can be cleared on one sweep (1/60 of a second).

The computer command word is strobed in through IC 47 which synchronizes the data valid line to the internal clock. IC 48 selects which of the four possible commands are going to be executed. If it is a crawl command the shift register, IC 44, is used to sequence the operations that can be performed in a single crawl command. The selectors IC 52 and 46 select which half of the sixteen bit command word is being utilized. The latch pair in IC 49 is used when the sixteen bit command word is to be interpreted as the absolute address of the cursor and activates the broadside load of the cursor counters, IC 3, 4, 25 and 26. Crawl commands simply increment or decrement these counters and are timed by IC 40.

The light pen generates a signal when the electron beam passes under a photo diode. This is shaped into a TTL signal and is used to latch ICs

16, 17, 41 and 42. IC 41 and 42 are simply tri-state latches that grab the vertical position of the electron beam when the light pen circuit hits. ICs 16 and 17 are tri-state latched counters that perform a similar function. However, the output of the counting chain (ICs 11, 12 and 13) are not exactly the horizontal address. The 8554's, (ICs 16 and 17) do count the horizontal address and latch it when the pen hit line goes low.

The memory is organized into an eight by eight matrix by the 8 chip enable lines and the 8 read/write lines. Data in and address lines are common to all chips. There are 8 data out lines which parallel the read/write lines and connect back to banks of 8 RAMS, only one of which is enabled by the chip enable signal. The low 3 bits of the data address are decoded to enable one of 8 blocks of 8 memory chips. Inexpensive 1 MHz 2102's can be used: eight are read simultaneously.

INTERFACING

Two typical computer hook-ups for the TV interface are described below for illustration. Users who follow these schemes will be able to easily use our software. The computer used is a S-100 based micro-computer with 24K RAM running under a CP/M disk operating system.

The first hook-up uses the IMSAI 4-P10 board. Two parallel output ports are used for a minimal configuration that permits use of the interface, but does not support all of its functions. Two ports are used, with bit assignments shown in Figure 6. In addition, an outboard circuit, shown in Figure 7 is required to generate a DATA VALID signal when the computer reads output data into port 10.

Use of a 3P+S board, such as manufactured by Processor Technology, permits full use of the interface and, in addition a keyboard, speaker, LED and serial device. This board can provide all the input/output functions required by the small computer system we have designed for educational use. Figures 8 and 9 show the complete I/O assignments for this computer including the TV interface.

In both configurations, DATA VALID is generated when Port 10 is addressed, so it is imperative to have the desired data previously loaded into Port 11. We find it convenient to leave Port 11 zeroed for crawl commands and issue commands, one at a time, to Port 10.

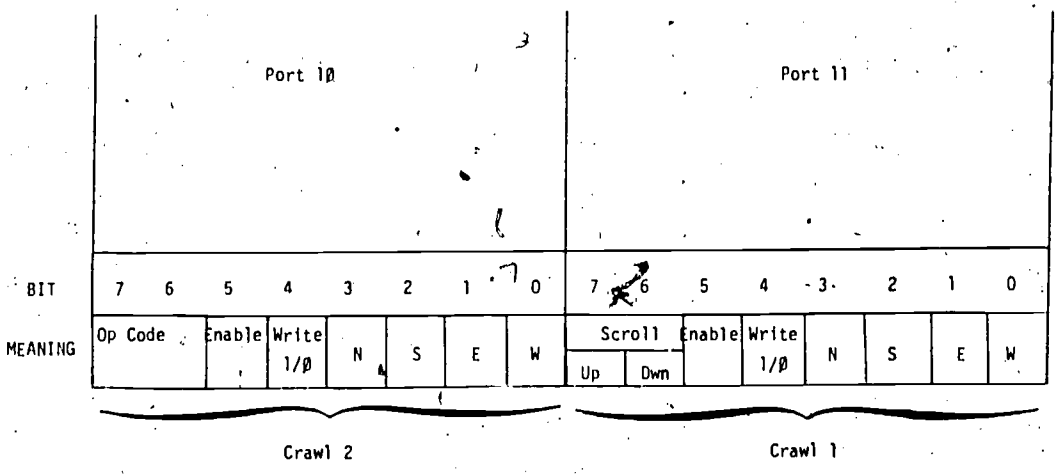
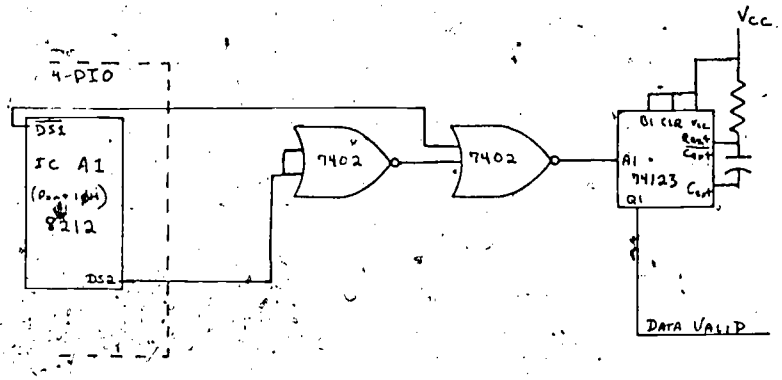


Figure 6. IMSAI 4-PIO
Port and bit assignments



$\overline{DS2}$ or $\overline{DS1}$ = DS1 and DS2

By using the A1 input on the 74123 one shot, the DATA VALID signal is generated on the falling edge of DS1 and DS2, at which time the data on the output ports is stable.

Figure 7. Outboard DATA VALID Generator

INPUT

PORT #	BIT #	DESIGNATION	MEANING	
10	0		KEYBOARD ASCII Code*	Keyboard Input
	1			
	2			
	3			
	4			
	5			
	6			
	7		KEYBOARD Strobe*	
11	0	P_0 P_8		Light Pen x and y input wired together
	1	P_1 P_9		
	2	P_2 P_{10}		
	3	P_3 P_{11}		
	4	P_4 P_{12}		
	5	P_5 P_{13}		
	6	P_6 P_{14}		
	7	P_7 P_{15}		
12	0	DAV	Receiver data available*	Status Register
	1	$\overline{VSYNC}$	Vertical sync	
	2	$\overline{BUT}$	Light pen button	
	3	B_1	bit 1	
	4	B_2	bit 2	
	5	FE	framing error*	
	6	PE	parity error*	
	7	XBMT	transmit buffer empty*	
13		UART * Data Input		

* Not needed for the TV Interface

Figure 8. 3P+S Input bit assignments

OUTPUT

PORT #	BIT #	DESIGNATION	MEANING	
11	0	D_8	W	Crawl 1
	1	D_9	E	
	2	D_{10}	S	
	3	D_{11}	N	
	4	D_{12}	Write I/O	
	5	D_{13}	Enable 12	
	6	D_{14}	Op Code low	
	7	D_{15}	Op Code high	
10	0	D_0	W	Crawl 2
	1	D_1	E	
	2	D_2	S	
	3	D_3	N	
	4	D_4	Write I/O	
	5	D_5	Enable 4	
	6	D_6	Scroll down	
	7	D_7	Scroll up	
12	0		Speaker*	Status
	1	PXEN	Enable light pen X address	
	2		Baud rate*	
	3		Status LED*	
	4		Parity*	
	5		Stop bits*	
	6		Word length 1*	
	7		Word length 2*	
13			UART Data Output*	

Note: DATA VALID is generated by OUTPUT STROBE B.
Also PYEN is obtained by inverting PXEN.

*Not needed for TV Interface.

Figure 9. 3P+S Output Bit Assignments

CONSTRUCTION

The interface has been reduced to three PC boards which are available at cost from TERC. In addition to the boards, the components listed in Table II are required.

Table III and IV list the number and type of each component to aid in locating them on the boards. The following Figures 10 and 11 show the actual parts placement on boards A and B. Board C is simply filled with the sixty-four 2102 memory chips and the eight .1 uf bypass capacitors.

Once populated, the boards need to be interconnected as described in the Wire Wrap List, Table V. The starred lines can be brought out and connected to the computer as suggested in the preceding section. The light pen must be added as an extra feature. Until we perfect our own design, we have been using a $50 pen made by Educational Data System of Virginia, Inc. (P.O. Box 2115, Newport News, VA 23602). Space for interfacing the light pen is provided on Board B. The circuit we use is shown in Figure 12.

TABLE II

Total Parts List - Video Interface Boards

Integrated Circuits

Chip Number	Quantity
7400	2
7402	1
7404	3
7405	1
7408	2
7410	2
7420	1
7430	1
7474	5
7486	1
74121	1
74151	1
74155	3
74157	6
74161	6
74164	1
74181	2
74193	6
74198	1
2102	64
8551	2
8554	2
74123	1

Resistors (1/8th watt)

Value	Quantity
470 Ohm	2
1K Ohm	11
10K Ohm	1
50K Ohm	1

Can be nearest standard value

Trimpots

10K Ohm	1
50K Ohm	1

Capacitors

Value	Quantity
10 pf	1
.1mfd disk	10
.22mfd	1
1 mfd	1

Miscellaneous

Part	Quantity
6Mhz X-tal	1
14 pin IC sockets	21
16 pin IC sockets	91
24 pin IC sockets	3

TABLE III

IC Identities and locations

Chip Number	on Board	Identity
1	A	74198
2	A	74151
3	A	74193
4	A	74193
5	A	7474
6	A	74157
7	A	74157
8	A	7408
9	A	7408
10	A	74155
11	A	74161
12	A	74161
13	A	74161
14	A	7430
15	A	7404
16	A	8554
17	A	8554
18	A	7402
19	A	7410
20	A	7486
21	A	7405
22	A	7404
25	B	74193
26	B	74193
27	B	74181
28	B	74181
29	B	74155
30	B	74157
31	B	74157
32	B	74193
33	B	74193
34	B	7410
35	B	74161
36	B	74161
37	B	74161
38	B	7404
39	B	7420
40	B	7400
41	B	8551
42	B	8551
43	B	7474
44	B	74164
45	B	7474
46	B	74157
47	B	7474
48	B	74155
49	B	7474
50	B	74121
51	B	7400
52	B	74157
53	B	74123

TABLE IV

VIDEO INTERFACE

Discrete Parts Placement

BOARD A

R7 through R11 — 1k

R12-470

R13-470

R14-10k pot

X1-6 mHz

BOARD B

R1 through R6 — 1k

R15-50k pot

R16-50k

R17-10k

C1-1 uf

C2-.22 uf

C3-10 pf

C4 through C13 — .1 uf disc

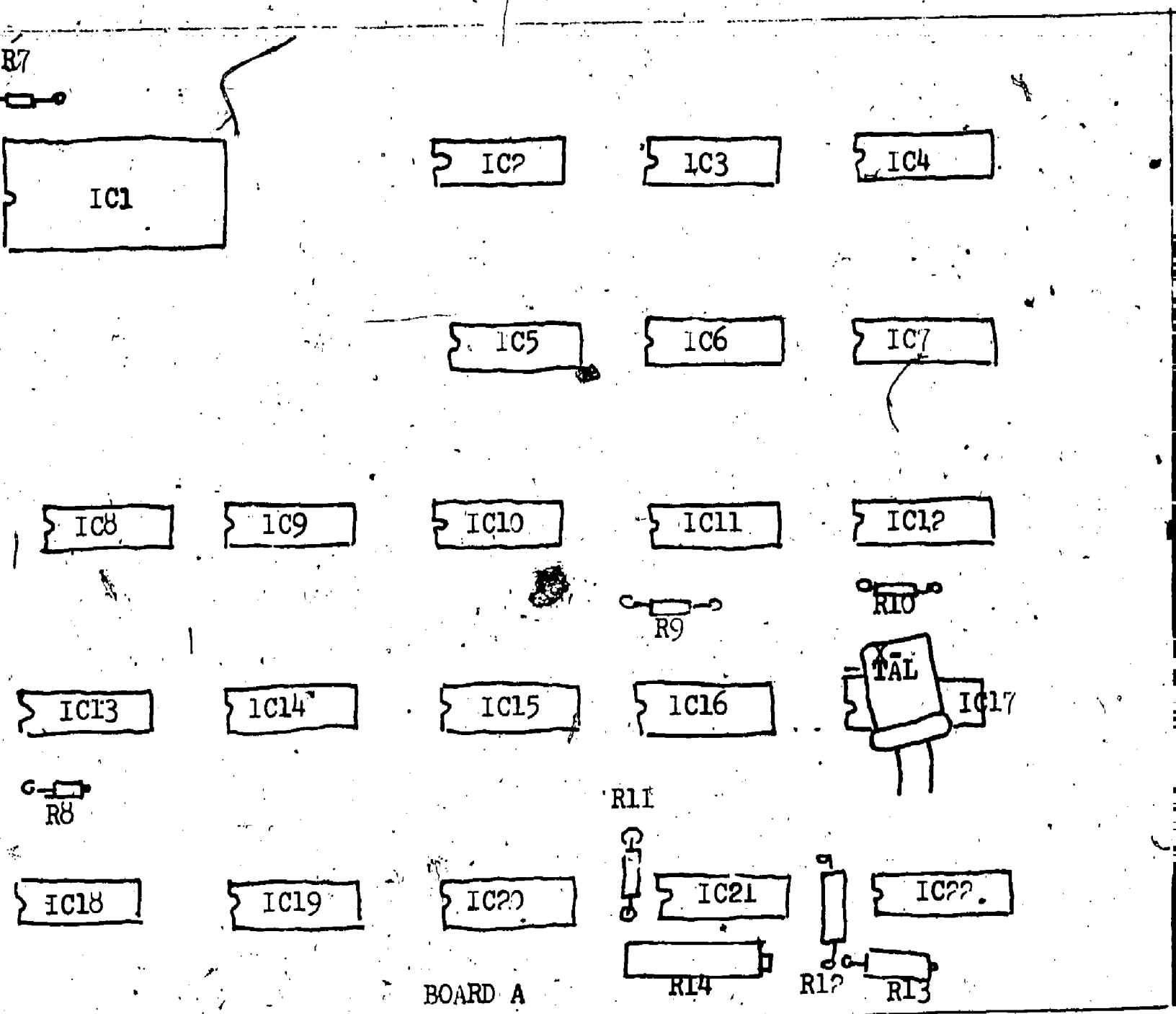


Figure 10. PARTS PLACEMENT - BOARD A

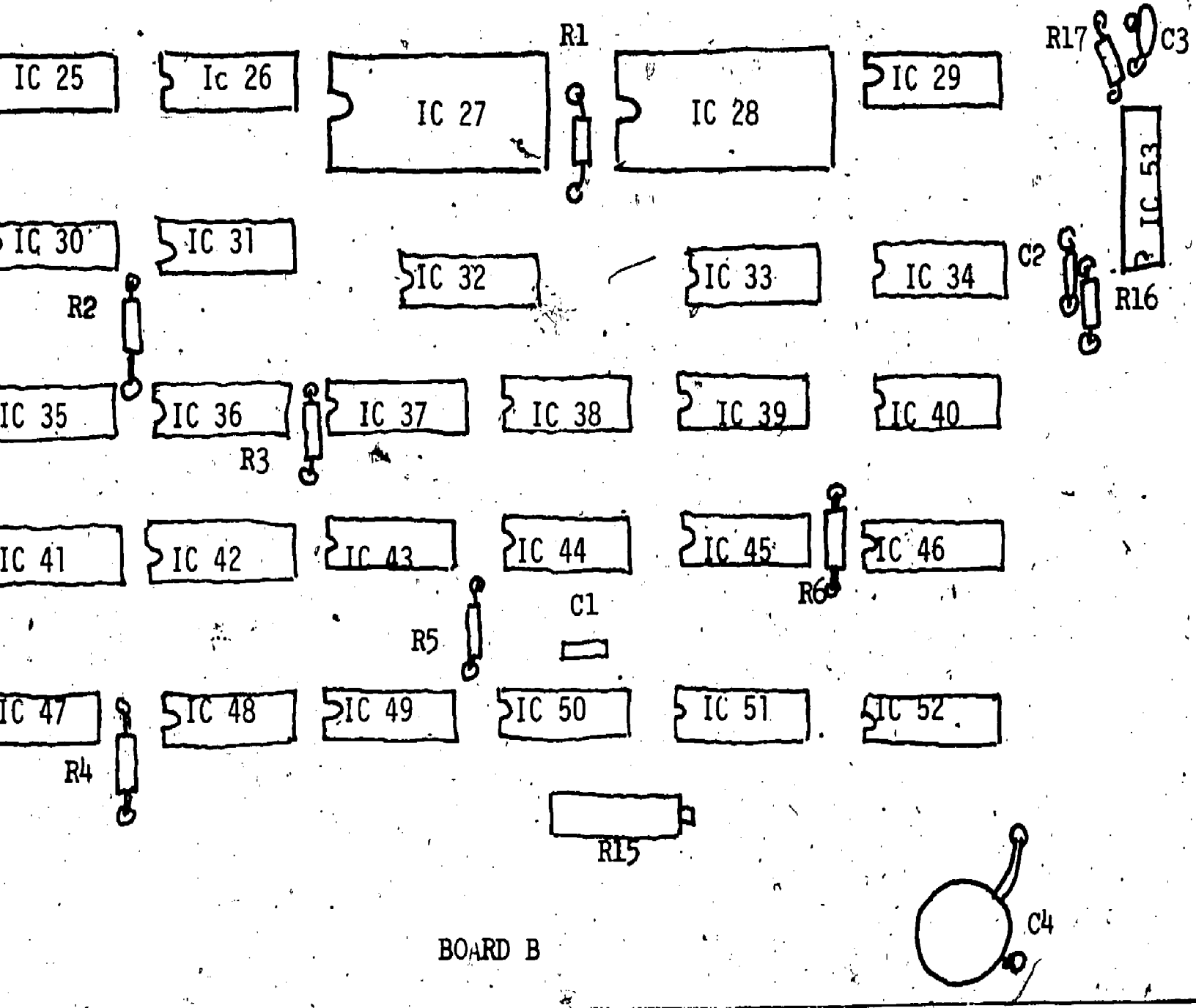


Figure 11. PARTS PLACEMENT - BOARD B

TABLE V

TV INTERFACE PC INTERCONNECTION

Wire Wrap List

Each of the three boards terminates in 72 pins which are numbered in the standard way. For the TV interface to operate correctly, a number of these pins need to be interconnected or brought our for external connections. The connections diagrams (Table V) on the following pages detail the connections that need to be made and the names of the signals that are brought out for interfacing to the TV or the computer. The Table shows the destination of each wire from each pin. The designation NC means no connection is necessary. For example, the first pin on Board A has no connection. The second pin on Board A is connected to Board C, pin 34 and is A_7, the seventh address line of the on-board memory. The fourth pin on Board A is connected to the 64th pin on Board B and is D_5, one of the wires which must be connected to the microcomputer to provide the input data word bit #5.

CONNECTIONS DIAGRAMS BOARD A

Pin #	Destination	Function
1)	NC	
2)	C-31	A-7
3)	NC	
4)	B-64	D_5*
5)	NC	
6)	B-49	6 MHz
7)	B-67, B30	$\overline{\text{pen hit}}$
8)	B-58	CC-1
9)	B-27	raster
10)		
11)	B-51, B-25	adr. load
12)	C-32	A-8
13)	B-46	D_7*
14)	C-30	A-9
15)	B-48	D_6*
16)	C-36	A-6
17)	B-62	D_4*
18)	C-38	A-5
19)	B-54	D_3*
20)	B-50	d. hold 1
21)	B-56	D_2*
22)		B_1
23)	B-60	D_0*
24)	B-52	d. hold 2
25)	B-57	h. inc.

Pin #	Destination	Function
26)		B_2*
27)	B-59	h. dec.
28)	B-55	$\overline{\text{write}}$
29)	C-14	data out 7
30)	B-53	$\overline{\text{busy-clear}}$
31)	C-16	data out 6
32)	C-58	w/r 4
33)	C-18	data out 5
34)	C-60	w/r 5
35)	C-20	data out 4
36)	C-64	w/r 7
37)	C-28	data out 0
38)	C-62	w/r 6
39)	C-26	data out 1
40)	C-56	w/r 3
41)	C-24	data out 2
42)	C-40	w/r 0
43)	C-22	data out 3
44)	C-52	w/r 1
45)	B-44	$\overline{\text{blank}}$
46)	C-54	w/r 2
47)	B-63	ID-74
48)	B-65	clock
49)	NC	
50)	C-51, B-68	ground
51)	B-61	background

Pin #	Destination	Function
52)		$\overline{\text{PXEN}}$ *
53)	B-26	$\overline{\text{vsync}}$
54)	B-45	P_4*
55)		$\overline{\text{hsync}}$
56)	B-35	P_1*
57)		video out*
58)	B-37	P_0*
59)	B-31	P_2*
60)	B-41	P_7*
61)	B-39	P_6*
62)	B-33	P_3*
63)	B043	P_5*
64)	NC	
65)	C-13, B-72	+5 V*
66)	NC	
67)	NC	
68)	NC	
69)	NC	
70)	NC	
71)	NC	
72)	NC	

*External Connections

CONNECTION DIAGRAMS BOARD B

Pin #	Destination	Function	Pin#	Destination	Function	Pin #	Destination	Function
1)	NC		26)	A-53	$\overline{\text{vsync}}$	52)	A-24	d. hold 2
2)	C-44	A-2	27)	A-9	raster	53)	A-30	$\overline{\text{BUSY}}$*
3)	NC		28)		DATA VALID*	54)	A-19	D_3*
4)	C-46	A-3	29)		$\overline{\text{PYEN}}$*	55)	A-28	$\overline{\text{write}}$
5)	NC		30)	A-7, B-67	pen hit*	56)	A-21	D_2*
6)	C-50	A-0	31)	A-59	P_{10}*	57)	A-25	h. inc.
7)	C-31	CE-4	32)	NC		58)	A-8	D_1*
8)		D_{13}*	33)	A-62	P_{11}*	59)	A-27	h. dec
9)	C-29	CE-5	34)	NC		60)	A-23	D_0*
10)		D_8*	35)	A-56	P_9*	61)	A-51	$\overline{\text{background}}$
11)	C-27	CE-6	36)	NC		62)	A-17	D_4*
12)		D_9*	37)	A-58	P_8*	63)	A-47	ID-74
13)	C-25	CE-7	38)	NC		64)	A-4	D_5*
14)		D_{12}*	39)	A-61	P_{14}*	65)	A-48	clock
15)	C-47	CE-0	40)	NC		66)	NC	
16)		D_{10}*	41)	A-60	P_{15}*	67)	A-7, B-30	$\overline{\text{pen hit}}$
17)	C-39	CE-1	42)	NC		68)	A-50, C-51	ground
18)		D_{11}*	43)	A-64	P_{13}*	69)	NC	
19)	C-35	CE-2	44)	A-45	$\overline{\text{blank}}$	70)	NC	
20)	C-42	A-1	45)	A-54	P_{12}*	71)		pen input
21)	C-33	CE-3	46)	A-13	D_7*	72)	A-65, C-43	+5 V
22)		D_{14}*	47)	C-37	data in			
23)	C-48	A-4	48)	A-15	D_6*			
24)		D_{15}*	49)	A-6	6 MHz			
25)	A-11, B-51	adr. load	50)	A-20	d. hold 1			
			51)	A-11, B-25	adr. load			

*External Connections

CONNECTION DIAGRAMS BOARD C

Pin #	Destination	Function
1)	NC	
2)	NC	
3)	NC	
4)	NC	
5)	NC	
6)	NC	
7)	NC	
8)	NC	
9)	NC	
10)	NC	
11)	NC	
12)	NC	
13)	NC	
14)	A-29	data out 7
15)	NC	
16)	A-31	data out 6
17)	NC	
18)	A-33	data out 5
19)	NC	
20)	A-35	data out 5
21)	NC	
22)	A-43	data out 3
23)	NC	
24)	A-41	data out2
25)	B-13	CE-7
26)	A-39	data out 1
27)	B-11	CE-6
28)	A-37	data out 0
29)	B-9	CE-5
30)	A-14	A-9
31)	B-7	CE-4
32)	A-12	A-8
33)	B-21	CE-3
34)	A-2	A-7
35)	B-19	CE-2
36)	A-16	A-6
37)	B-47	data in
38)	A-18	A-5
39)	B-17	CE-1
40)	A-42	r/$\overline{w}$ 0
41)	NC	
42)	B-20	A-1
43)	A-65, B-72	+5 V
44)	B-2	A-2
45)	NC	
46)	B-4	A-3
47)	B-15	CE-0
48)	B-23	A-4
49)	NC	
50)	B-6	A-0
51)	A-50, B-68	ground
52)	A-44	r/$\overline{w}$ 1
53)	NC	
54)	A-46	r/$\overline{w}$ 2
55)	NC	
56)	A-40	r/$\overline{w}$ 3
57)	NC	
58)	A-32	r/$\overline{w}$ 4
59)	NC	
60)	A-34	r/$\overline{w}$ 5
61)	NC	
62)	A-38	r/$\overline{w}$ 6
63)	NC	
64)	A-36	r/$\overline{w}$ 7
65)	NC	
66)	NC	
67)	NC	
68)	NC	
69)	NC	
70)	NC	
71)	NC	
72)	NC	

*External Connections

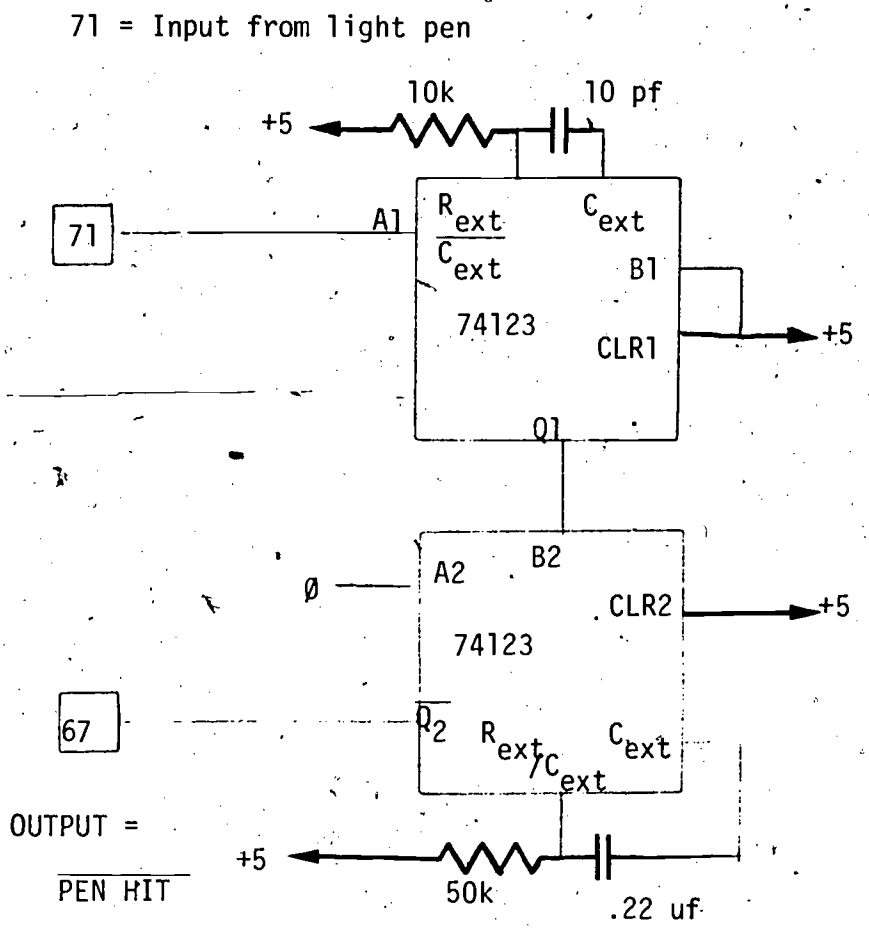


Figure 12. Light Pen Interface on Board B.